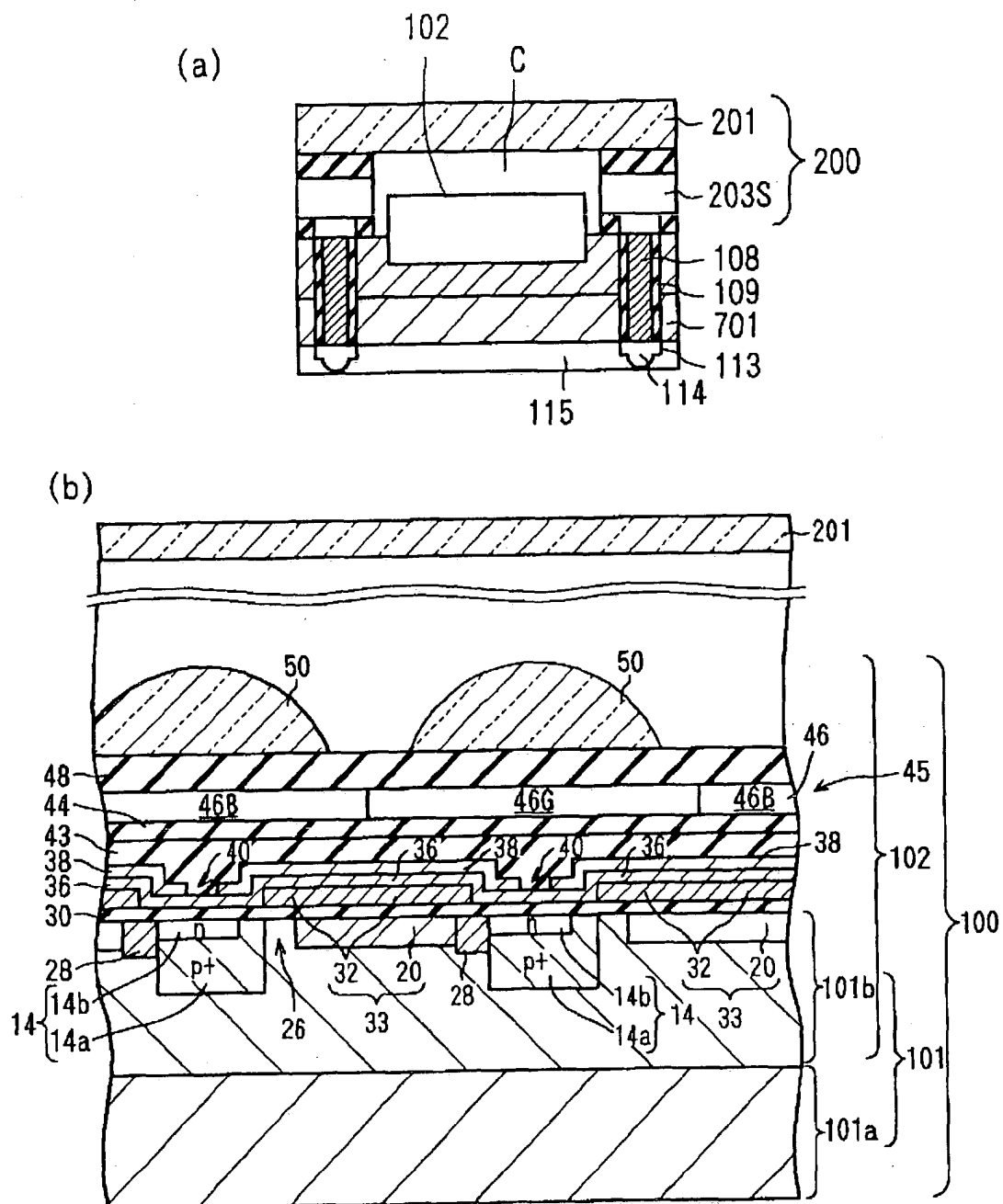
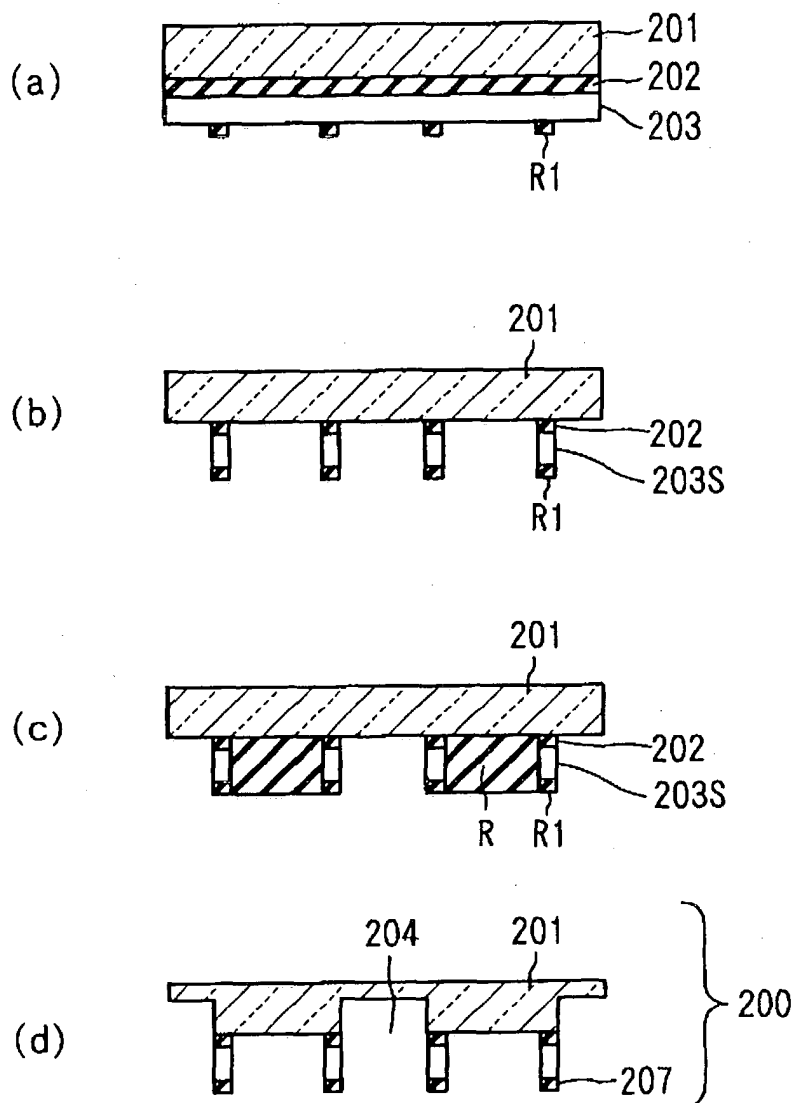


【書類名】 図面

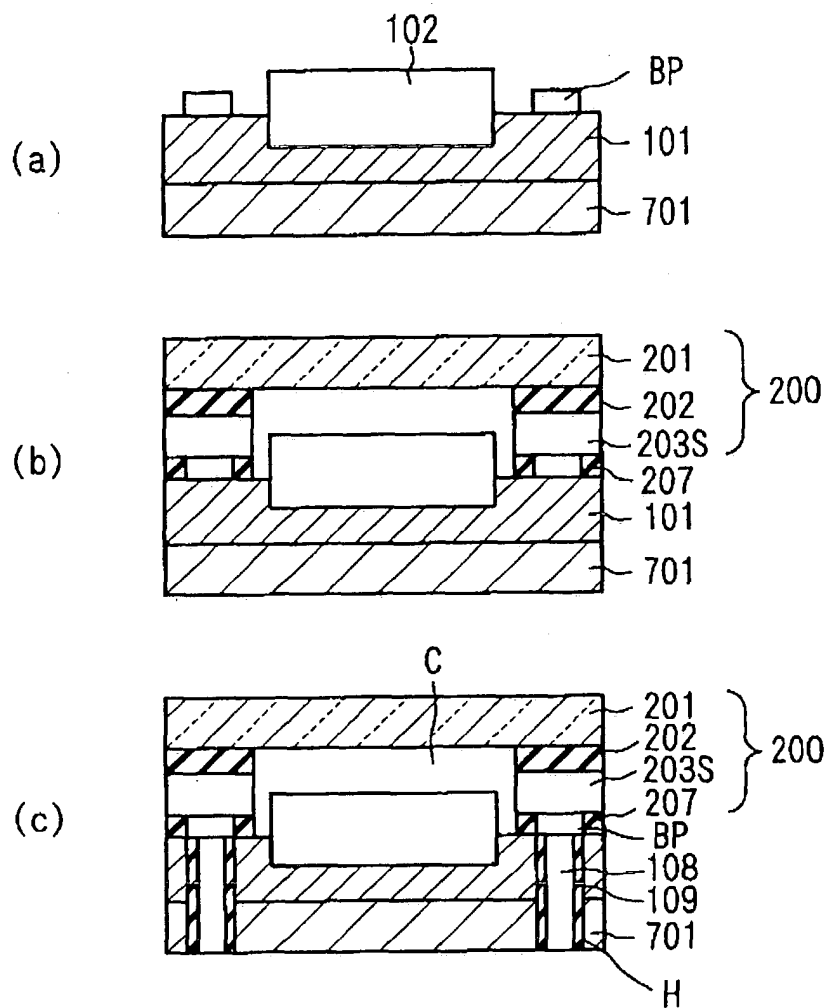
【図 1】



【図 2】



【図 3】



【図 4】

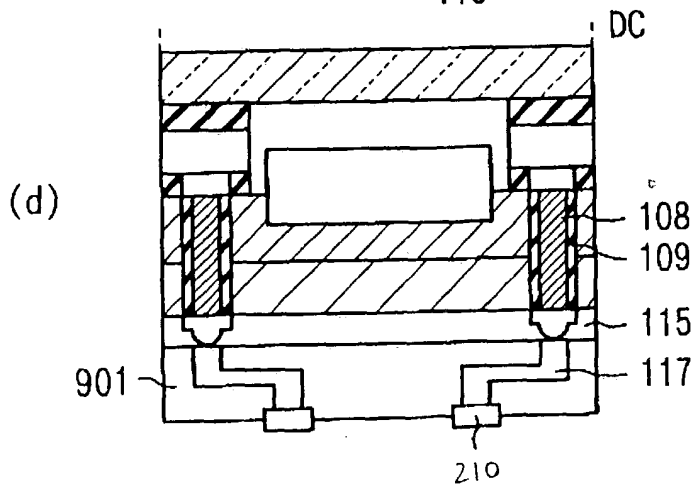
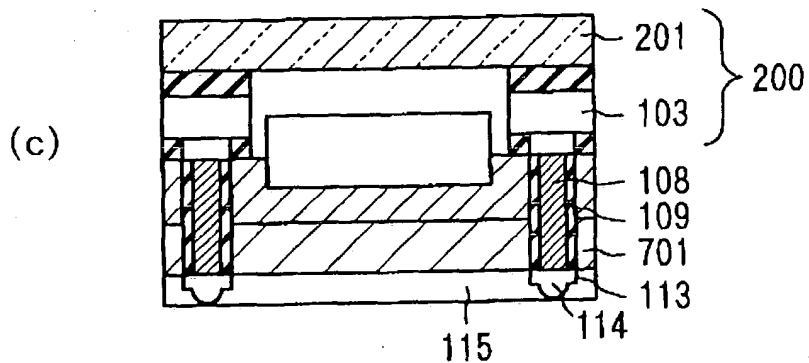
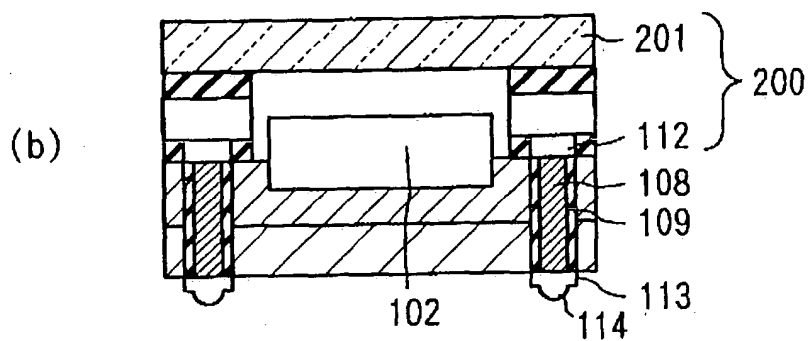
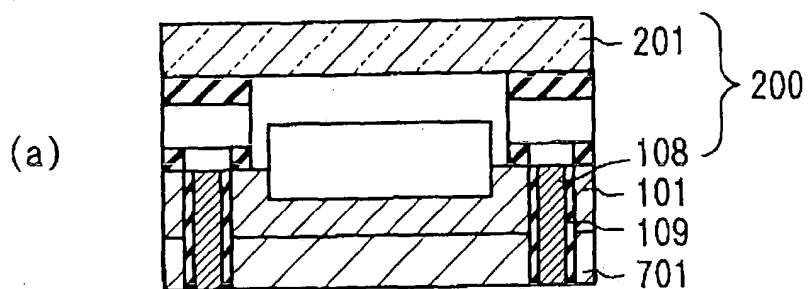
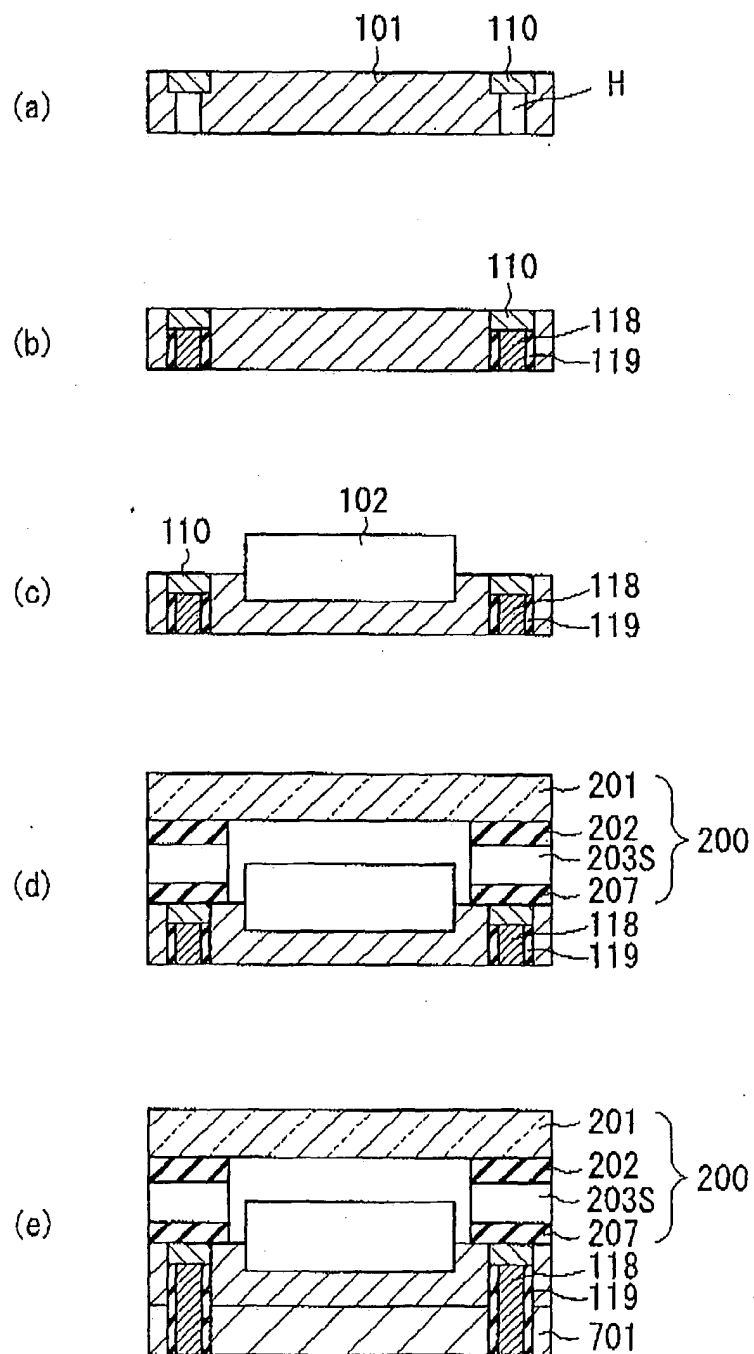


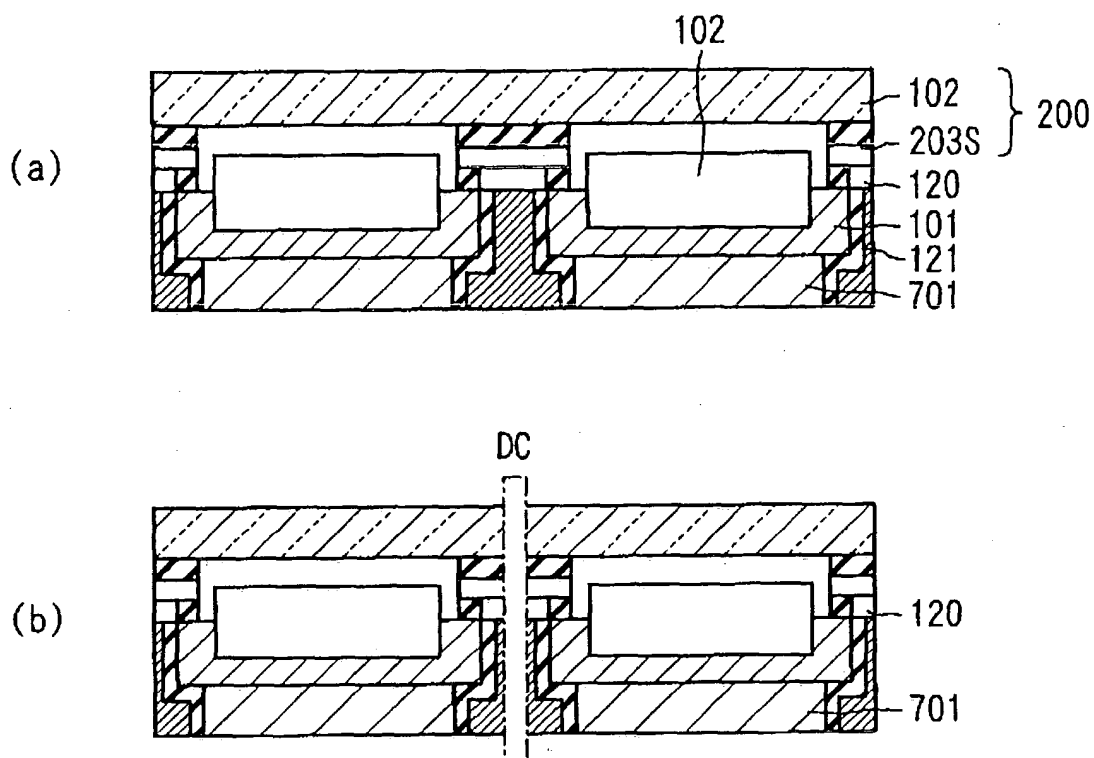
Figure 1 consists of five cross-sectional views of a semiconductor device, labeled (a) through (e), illustrating the manufacturing process:

- (a) A substrate 101 with two openings. Each opening contains a plug 110. A layer 118 is formed on top of the substrate and plugs.
- (b) A layer 119 is formed on top of layer 118. The top surface of layer 119 is planarized with the top surface of layer 118.
- (c) A rectangular block 102 is formed on top of layer 119. The top surface of block 102 is planarized with the top surface of layer 119.
- (d) A multi-layered structure 200 is formed on top of block 102. The layers of structure 200, from top to bottom, are 201, 202, 203S, and 207. The top surface of layer 207 is planarized with the top surface of layer 119.
- (e) A layer 701 is formed on top of layer 207. The top surface of layer 701 is planarized with the top surface of layer 119. A layer 108 is formed on top of layer 701.

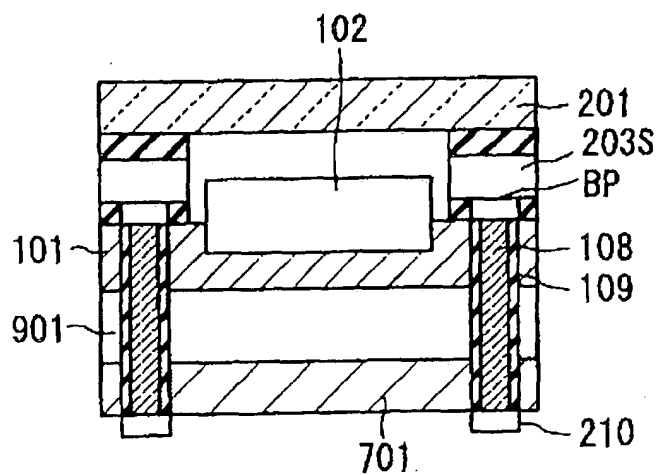
【図 6】



【図 7】



【図 8】



【図9】

